We claim:

1. A programmable processor comprising:

an instruction path;

a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a cache operable to retain data communicated between the external interface and the data path;

a register file operable to receive and store data from the data path and communicate the stored data to the data path; and

an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single instruction specifying both a shift amount and a register having a register width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the number of data elements in the first plurality of data elements being inversely related to the elemental width, the shift amount configurable to an amount inclusively between zero and one less than the elemental width, the execution unit is operable to:

(i) shift a subfield of each of the first plurality of data elements by the shift amount to produce a second plurality of data elements; and

(ii) provide the second plurality of data elements as a catenated result.

2. The processor of claim 1 wherein the catenated result is provided to a register.

3. The processor of claim 1 wherein the shift amount is contained in a register specified by the instruction.

4. The processor of claim 1 wherein the shift amount is contained in an immediate field of the instruction.

5. The processor of claim 1 wherein each data element in the first plurality of data elements has a sign bit in a most significant bit position and wherein the execution unit is further operable to fill a shift amount number of most significant bits in each of the second plurality of data elements with the sign bit from a respective data element in the first plurality of data elements.

6. The processor of claim 1 wherein the execution unit is further operable to fill a shift amount number of most significant bits in each of the second plurality of data elements with zeros.

7. The processor of claim 1 wherein the execution unit is further operable to fill a shift amount number of bits in each of the second plurality of data elements with a subfield from a respective location of the contents of an additional register.

8. The processor of claim 1 wherein the catenated result has a width of 128 bits.

9. The processor of claim 1 wherein the elemental width of each of the first plurality of data elements is 32 bits.

10. The processor of claim 1 wherein the elemental width of each of the first plurality of data elements is 16 bits.

11. The processor of claim 1 wherein an elemental width of each of the second plurality of data elements is equal to the elemental width of each of the first plurality of data elements.

12. The processor of claim 1 wherein an elemental width of each of the second plurality of data elements is equal to twice the elemental width of each of the first plurality of data elements.

13. The processor of claim 1 wherein an elemental width of each of the second plurality of data elements is equal to half the elemental width of each of the first plurality of data elements.

14. A method for shifting data in a programmable processor, the method comprising:

decoding a single instruction specifying both a shift amount and a register having a register width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the number of data elements in the first plurality of data elements being inversely related to the elemental width, the shift amount configurable to an amount inclusively between zero and one less than the elemental width;

shifting a subfield of each of the first plurality of data elements by the shift amount to produce a second plurality of data elements; and

providing the second plurality of data elements as a catenated result.

15. The method of claim 14 wherein the catenated result is provided to a register.

16. The method of claim 14 wherein the shift amount is contained in a register specified by the instruction.

17. The method of claim 14 wherein the shift amount is contained in an immediate field of the instruction.

18. The method of claim 14 wherein each data element in the first plurality of data elements has a sign bit in a most significant bit position and wherein the method further comprises:

filling a shift amount number of most significant bits in each of the second plurality of data elements with the sign bit from a respective data element in the first plurality of data elements.

19. The method of claim 14 wherein the method further comprises:

filling a shift amount number of bits in each of the second plurality of data elements with zeros.

20. The method of claim 14 wherein the method further comprises:

filling a shift amount number of bits in each of the second plurality of data elements with a subfield from a respective location of the contents of an additional register.

21. The method of claim 14 wherein the catenated result has a width of 128 bits.

22. The method of claim 14 wherein the elemental width of each of the first plurality of data elements is 32 bits.

23. The method of claim 14 wherein the elemental width of each of the first plurality of data elements is 16 bits.

24. The method of claim 14 wherein an elemental width of each of the second plurality of data elements is equal to the elemental width of each of the first plurality of data elements.

25. The method of claim 14 wherein an elemental width of each of the second plurality of data elements is equal to twice the elemental width of each of the first plurality of data elements.